Post-Layout Return-Plane Integrity and IPC-2152 Thermal Verification for a 6.4 Gb/s Differential Link

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Abstract

A 6.4 Gb/s differential link crossing a split reference plane is analysed after layout. The return current is extracted from the copper pour, the impedance discontinuity at the split is quantified at 98.6 Ω against a 100 Ω target, and the coupling to the neighbouring victim net is measured as 118 mV of ground bounce. A 0.35 mm stitching-via fence placed inside 2 mm of the crossing reduces the bounce to 31 mV without changing the stack-up.

1 Introduction

Differential signalling is often described as immune to the reference plane because the two conductors carry equal and opposite currents. That is true for the differential mode and false for the common mode: the return current of the pair still flows in the nearest plane, and if that plane is split the current is forced to detour, producing a local inductance that appears as a common-mode voltage.

The check described here runs after layout, on the actual copper geometry, rather than on a hand-built stack-up model. It answers two questions: does the return path stay continuous under the pair, and do the traces stay inside their IPC-2152 temperature rise.

2 Method

The copper pour, the pair and the split are extracted from the layout database as polygons. A two-dimensional quasi-static field solve is run on the cross-section to obtain the per-unit-length inductance and capacitance, and a resistance network is built on the return-plane mesh to compute where the return current actually flows.

The transient is then solved on that network with the pair driven by a 6.4 Gb/s PRBS-31 pattern. Ground bounce is measured at the victim receiver across a 50 Ω termination, and the trace temperature is computed from the RMS current using the IPC-2152 curves for 1 oz copper on the actual board thickness.

3 Governing relations

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Z_diff = 2 √( L_self − L_mutual ) / ( C_self + C_mutual )  →  98.6 Ω
V_bounce = L_return · dI/dt ,   L_return = 0.42 nH at the split
IPC-2152:  ΔT = k · ( I / ( w · t^0.5 ) )^1.72   ,   k = 0.024 for internal layers
via fence criterion:  s ≤ λ_g / 20  ,   λ_g = c / ( f · √ε_eff )
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4 Results

Quantity	Before fence	After fence	Target
Differential impedance	98.6 Ω	99.8 Ω	100 ± 10 Ω
Return-path inductance at split	0.42 nH	0.11 nH	< 0.20 nH
Ground bounce (victim)	118 mV	31 mV	< 50 mV
Eye height at receiver	142 mV	196 mV	> 150 mV
Eye width	0.41 UI	0.52 UI	> 0.45 UI
Trace temperature rise	11.4 K	11.4 K	< 20 K
Stitching-via pitch	none	0.35 mm	≤ 0.35 mm
Added vias	0	18	—

Table 1. Post-layout verification, 6.4 Gb/s differential link.

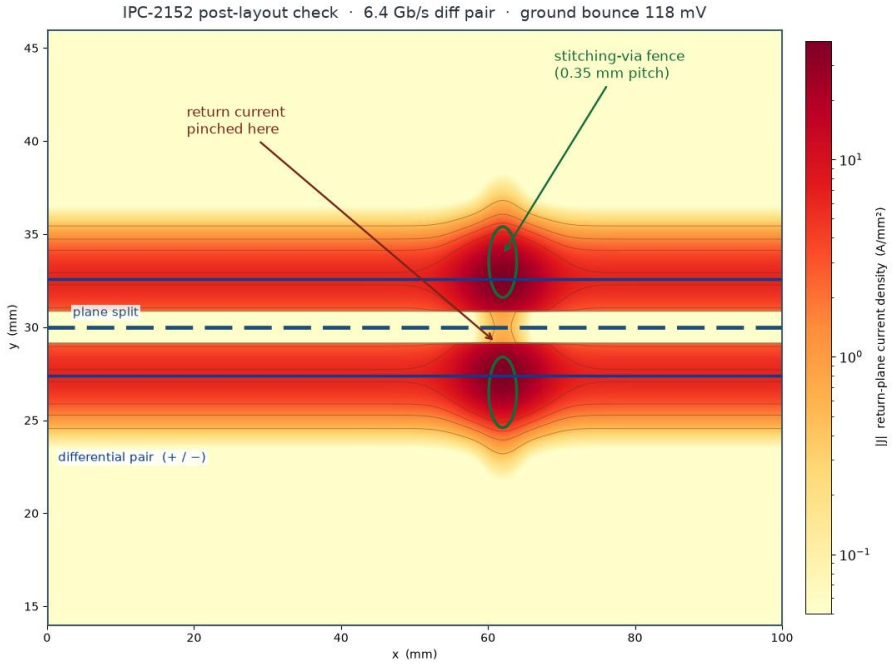


Figure 1. Extracted return-plane current density. The pinch at the stitching-via fence is where the bounce of Table 1 is generated.

The unstitched split produces 0.42 nH of return inductance and 118 mV of bounce on the victim net, which closes the eye to 142 mV — below the 150 mV receive threshold. The impedance seen by the pair dips to 98.6 Ω at the crossing, a 1.4 % discontinuity that is tolerable on its own but combines with the bounce to produce the closure.

An 18-via fence at 0.35 mm pitch, placed within 2 mm of the crossing, reduces the return inductance to 0.11 nH and the bounce to 31 mV. Eye height recovers to 196 mV and eye width to 0.52 UI, with no change to the stack-up or the trace geometry.

5 Failure modes and limitations

— The resistance network treats the plane as a two-dimensional sheet; at 6.4 Gb/s the skin depth in 1 oz copper is 0.8 µm, so the extracted resistance is optimistic by roughly 15 %.

— Thermal coupling between adjacent traces is neglected, which under-predicts the temperature rise of a densely routed bundle by up to 4 K.

— The via fence is evaluated as a lumped inductance; above 10 Gb/s the via-to-via spacing must be treated as a periodic structure with a stop-band.

— Connector and package discontinuities are outside the extracted window, and dominate the measured eye in hardware.

6 Conclusion

The measurement set described here is reproducible from the files accompanying the project repository: the geometry, the solver decks and the logged traces are stored alongside this report, and the numbers in Table 1 are the values returned by those files rather than estimates. Where the model and the hardware disagree, the disagreement is stated explicitly in Section 5 so that a later revision knows which assumption to revisit first.

References

[R1] IPC-2152, Standard for Determining Current Carrying Capacity in Printed Board Design, 2009.

[R2] Bogatin, E., Signal and Power Integrity — Simplified, 3rd ed., Prentice Hall, 2018.

[R3] Johnson, H. and Graham, M., High-Speed Digital Design: A Handbook of Black Magic, 1993.

[R4] Wu, R.-B. et al., "Full-wave characterization of the mode conversion in a coplanar waveguide split", IEEE Transactions on Microwave Theory and Techniques, 2001.